WHAT IS CLAIMED IS:

1. A test apparatus for testing a plurality of semiconductor devices loaded on one handler connected to a tester, the handler comprising:

a head board containing at least first and second sites on which semiconductor devices can be loaded for testing; and

a test head to generate site selection signals corresponding to different head board sites for sequential test cycles;

wherein semiconductor devices loaded on the first site are tested in response to one site selection signal, and semiconductor devices loaded on the second site are tested in response to another site selection signal.

2. The test apparatus of claim 1, wherein the test head counts test cycles provided from the tester to generate different site selection signals.

3. The test apparatus of claim 1, wherein the test head includes a plurality of fuses, wherein different fuses are selectively shorted to a power supply voltage to selectively generate different site selection signals.

4. The test apparatus of claim 1, wherein the handler has the capability to sort, according to a test result obtained for the first head board site, semiconductor devices loaded on the first site while semiconductor devices loaded on the second head board site are selectively tested in response to the site selection signal corresponding to the second head board site.

5. A test apparatus for testing a plurality of semiconductor devices loaded on one handler connected to a tester, the handler comprising:

at least first and second head boards on which semiconductor devices can be loaded for testing; and

a test head to generate selection signals corresponding to different head boards for sequential test cycles;

wherein semiconductor devices loaded on the first head board are tested in response to one selection signal, and semiconductor devices loaded on the second head board are

tested in response to another selection signal.

6. The test apparatus of claim 5, wherein the test head counts test cycles provided from the tester to generate different selection signals.

7. The test apparatus of claim 5, wherein the test head includes a plurality of fuses, wherein different fuses are selectively shorted to a power supply voltage to selectively generate different selection signals.

8. The test apparatus of claim 5, wherein the handler has the capability to sort, according to a test result obtained for the first head board, semiconductor devices loaded on the first head board while semiconductor devices loaded on the second head board are selectively tested in response to the selection signal corresponding to the second head board.

9. A method of testing a plurality of semiconductor devices loaded on one handler connected to a tester, the method comprising:

loading semiconductor devices on two or more sites of the handler;

transmitting a test-require signal from the handler to the tester;

responding to the test-require signal with a query to the handler as to whether the semiconductor devices are all loaded on a fullsite;

in response to the handler query, generating a site selection signal corresponding to one of the handler sites;

testing the semiconductor devices loaded on the selected handler site in response to the site selection signal; and

sorting the semiconductor devices according to the test result of the selected handler site, while conducting another test cycle of another handler site.

10. The method of claim 9, wherein generating a site selection signal comprises selectively shorting a power supply voltage to a selected handler site through a fuse.

11. The method of claim 9, wherein generating a site selection signal comprises responding to a test cycle clock signal by activating a next site selection signal in a defined site selection signal sequence.